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Defects and Impurities in 4H- and 6H-SiC Homoepitaxial Layers: Identification, Origin, Effect on Properties of Ohmic Contacts and Insulating Layers and Reduction

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A chemical vapor deposition system has been designed and is being constructed for the purpose of depositing 4H- and 6H-SiC and AlN thin films. The design incorporates a separate load lock from which the growth chamber and a RHEED chamber are attached. Comparisons between the wetting characteristics of 6H-SiC(0001)Si and Si(111) surfaces in various acids and bases were conducted. The 10:1 HF dipped Si(111) surfaces were hydrophobic; the (0001)Si 6H-SiC surfaces were hydrophilic. The 6H-SiC(0001)Si surfaces capped with a 20Å Si layer, however, were hydrophobic after HF dipping and exhibited outgassing levels on annealing which were several orders of magnitude lower than SiC wafers dipped in HF without the capping layer. Annealing the Si capped (0001)Si 6H-SiC surfaces in UHV at 1100°C for 5 min. caused thermal desorption of the Si capping layer and the formation of a (3×3) Si rich, oxygen free (0001)Si 6H-SiC surface. As-deposited (at RT) NiAl, Au, and Ni contacts were rectifying on p-type 6H-SiC (0001) with very low leakage current densities (~1×10^{-8} A/cm^2 at 10 V). The Schottky barrier heights showed a reduced dependence on the metal work functions, a result which is in agreement with those for n-type SiC. Ni/NiAl contacts on p+ (1×10^{19} cm^{-3}) SiC were ohmic after annealing for 10–80 s at 1000°C in a N_2 ambient. The estimated specific contact resistivity was 2–3×10^{-2} W•cm^2. The high contact resistivities are partly attributed to an insulating oxide layer which formed at the surface of the contacts during the annealing process. Cr-B contacts were semi-ohmic on p-type SiC (1×10^{18} cm^{-3}) after annealing at 1000°C for 60–300 s in Ar; oxidation of these latter contacts did not occur. A three-step, integrated, UHV compatible, surface preparation, initial insulator formation, and oxide deposition process system is being developed for oxide growth on 6H-SiC. This system will be integrated with an advanced characterization facility which will allow various *in vacuo* characterization of the resulting oxides followed by I-V and C-V characterization. A special mask set has been employed to fabricate MOS capacitors and MOS gated diodes to enable accurate characterization of the SiO_2-SiC interface. N^+ implantation and active regions have been defined.

14. SUBJECT TERMS
4H-SiC, 6H-SiC, silicon carbide, AlN, chemical vapor deposition, thin films, ohmic contacts, Schottky barrier heights, work function, NiAl, Cr-B, contact resistivity, wetting, hydrophobic, hydrophilic, thermal desorption, oxide deposition, I-V, C-V, SiO_2-SiC interface MOS capacitors, MOS gated diodes

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I. Introduction

The two most important materials-related problems affecting the performance of all SiC devices and their associated components (e.g., contacts) are the defects and the undesired impurities which become incorporated in the homoepitaxial SiC layers in which all devices are currently fabricated. Bhatnagar [1] has shown that the reverse blocking leakage current in high voltage Schottky diodes is three orders of magnitude higher than theoretically predicted as a result of defects in the epi-layer. The formation of micropipes, stepped screw dislocations, interacting dislocation loops, polyganized networks of dislocations and growth twins as well as stacking faults during the sublimation growth of SiC boules are likely the root cause of some of the defects in the epitaxial layer. However, with the exception of the micropipes, the types and concentrations of line, planar and other three-dimensional defects and their effect on the performance of devices and individual device components in the important epi-layer have not been similarly determined. As such, it is not known which of the latter defects actually are translated from the wafer into the epi-layer during its deposition and, therefore, should be vigorously controlled during boule growth and which defects are generated during deposition.

The relatively uncontrolled occurrence of the n-type donor of N and deep level compensating impurities such as Ti in the epilayer have been identified via secondary ion mass spectrometry, photoluminescence and cathodoluminescence investigations. However, the origins of essentially all of these impurities are unknown. For high-temperature, -power and -frequency devices, it is highly desirable to control or eliminate these impurities such as to attain undoped films with uncompensated carrier concentrations of 10^{14} cm^{-3}—two orders of magnitude lower than what is, at present, normally achieved in standard commercial depositions.

The formation of low resistivity and thermally stable ohmic contacts to 4H- and 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have an advantage over Si, the contact resistivities must be below 1×10^{-5} Ω-cm^2, as noted by Alok, *et al.* [2]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on low melting point Al or Al alloys to dope the SiC surface below the contacts. These materials are not suitable for devices intended for high-temperature operation. While the fabrication of ohmic contacts to SiC has also normally depended on the attainment of a very heavily-doped near-surface region, the introduction during deposition of high levels of dopants in the near surface device region of the epi-layer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice.

Based on all of these issues and recent experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

To fabricate most microelectronic devices, the growth or deposition of stable insulators is needed to provide both passivating layers and gate dielectrics. Silicon carbide is almost invariably thermally oxidized, albeit at a slower rate, in the same manner and temperature range that is employed for Si. Most of the previous studies regarding the oxidation of SiC have been concerned with polycrystalline materials. It has been shown by Harris and Call [3] and Suzuki, *et al.* [4] that the (0001) face of 6H-SiC oxidizes according to the same linear-parabolic equation reported for Si by Deal and Grove [5]. The model states that the initial stage of oxidation is reaction rate limited and linear, but becomes parabolic as the diffusion of the oxidant through the oxide becomes the rate limiting factor. Research at NCSU by Palmour *et al.* [6] has demonstrated that the oxidation process on SiC in wet and dry oxygen and wet argon obeys the linear-parabolic law. Both wet processes had a slower rate than dry oxidation at 1050°C and below. The dry oxides exhibited a very flat surface; in contrast, SEM and TEM revealed that wet oxidation preferentially oxidizes dislocation bands, causing raised lines on the oxide and corresponding grooves in the SiC. It was proposed that the much higher solubility of H_2O in SiO_2 as compared to that of O_2 allows wet oxidation to be preferential.

All of the oxidation studies on all polytypes of semiconductor quality SiC have been conducted on n-type material with the exception of the investigation by Palmour *et al.* [6]. The objective of this study was the determination of the redistribution of the common electrical dopants of N, P, Al and B during thermal oxidation of SiC films at 1200°C in dry O_2. Experimental segregation coefficients and interfacial concentration ratios were determined. Secondary ion mass spectrometry revealed that B and Al depleted from the SiC into the growing oxide while N and P were found to pile up in the SiC as a result of the loss of the SiC to the oxide formation. Aluminum is now used almost universally as the p-type dopant in SiC. The electrical properties of oxides thermally grown on n-type SiC normally have reasonably favorable characteristics of high breakdown voltage and low leakage currents. However, the reverse is true for thermally grown oxides on p-type SiC, as shown by Baliga and his students at NCSU. It is believed that at least two of the causes of the poor performance on a p-type material are the existence of the Al in the oxide and at the oxide/SiC interface and the dangling oxygen bonds which this species creates in the oxide as a result of a difference in oxidation state (+3) compared to that of Si (+4) and the existence of C at the SiC/insulator interface. Methods of effectively cleaning SiC surfaces prior to oxidation to deposit and grow oxides on p-type material under UHV conditions and determine the effect of Al redistribution and C concentrations at the interface on the properties of the oxide must be determined. In addition,

the effect of existing line and planar defects in the SiC epi-layer on the properties of the thermally grown and deposited oxide must be ascertained.

The research conducted in this reporting period and described in the following sections has been concerned with (1) design and construction of a new CVD SiC system for the deposition of 6H- and 4H-SiC and AlN films, (2) studies of *ex situ* cleaning of the Si(111), 6H-SiC(0001) and Si-coated 6H-SiC(0001) surfaces in HF, (3) deposition, annealing and electrical characterization of Ni, NiAl, Au and Cr-B contacts to p-type SiC, (4) design and fabrication of a new, UHV-compatible and integrated system of *in situ* cleaning, oxidation and oxide deposition on SiC and its integration with characterization equipment, and (5) the design and use of a special mask set to fabricate metal oxide-semiconductor capacitors and gated diodes to enable accurate characterization of the SiO_2-SiC interface. The following individual sections detail the procedures, results, discussions of these results, conclusions and plans for future research. Each subsection is self-contained with its own figures, tables and references.

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II. Design and Construction of Silicon Carbide Chemical Vapor Pressure Deposition System

A. Introduction

A silicon carbide system has been designed and is being built in order to grow silicon carbide and aluminum nitride thin films of high quality. Currently, many parts have been received, and others are on order to obtain the necessary components for the proposed system.

B. Experimental Procedure

The system design is comprised of a six-way cross, serving as a loadlock, from which two separate chambers are attached. On one side of this loadlock is a growth chamber. To another side, perpendicular to the axis of the loadlock and growth chamber, is another chamber, where RHEED analysis will be performed. The sample will be transferred to and from the various chambers on a SiC-coated graphite susceptor platform on which the sample will be placed. The transfer mechanism consists of a platform which is moved from chamber to chamber by means of a manipulator rod, which is screwed to the side of the susceptor.

The growth chamber consists of a rotating module, to which the susceptor is attached. Growth will occur on the sample in an upside-down position, with gases flowing upward, while the susceptor is being rotated. The susceptor is attached to the rotating rod assembly by a groove into which the susceptor slides when transfer of the sample occurs. Once the sample is transferred to the rotating rod, the rod is brought down to the quartz portion of the reaction. Here, the sample is heated via RF coil, and gases are introduced from the bottom of the reactor. Growth temperature will be monitored by means of a standing pyrometer mounted outside the quartz chamber, aimed at the sample. Growth processes, such as gas flow rate and pressure, will be monitored by electronic components. Gas flow will be controlled by mass flow controllers, and pressure by capacitance manometers.

The RHEED (reflection high-energy electron diffraction) chamber, attached on another side of the loadlock chamber, will monitor film crystallinity, crystal structure and the formation of new surfaces. Since the growth of high-quality crystalline SiC films is being attempted, a RHEED chamber which is attached to a nominal high vacuum to prevent direct exposure to atmosphere after growth will be useful to characterize the film.

The SiC growth process will consist of introducing SiH_4 and C_2H_4 as the reactive components carried by a H_2 carrier. Nominal flow values will be on the order of 1 to 10 sccm for each. H_2 carrier flows will be on the order of 3 liters per minute. Other gases which will be included on the system will be NH_3 and an N_2/H_2 mixture, for doping, and Ar. TEA will also be used for doping, which will be kept at constant temperature by a heater bath.

C. Results

To date, a design has been developed where sample transfer, growth, and RHEED analysis have been determined. In addition, a support frame to provide physical support to the system has been designed and built. Three six-way crosses have been put together with the adjoining gate valves on the frame, and available flanges and window ports have been attached. Also, a quartz chamber-to-cross assembly has been machined, which will provide a sealed interface between two parts of the growth chamber. Quartz cylinders have been cut to design dimensions

Flange parts, pressure gauge attachments, pump connection parts, and a rotating rod assembly, are currently either being machined, or are on order, as are a manipulator stage, RHEED gun parts, and an optical pyrometer. An RF generator has been refurbished and is currently being returned to us to be used to provide RF heating of the susceptor.

D. Discussion

The proposed design was developed with many sources of input. A number of constraints determined the design configuration and materials used in the system.

One of the main concerns is the high operating temperature of the growth chamber. Since temperatures around 1600-1700°C are going to be used to grow SiC thin films, it was determined that quartz would be the best material for the growth portion of the chamber. Once this was determined, a design had to be developed to cool the chamber. A double-walled quartz vessel, water cooled around the perimeter, was determined to be the optimum mode of cooling.

Another concern is the transfer mechanism of the susceptor and the placement of samples on the susceptor surface. It was decided that small silicon carbide screws would be the most flexible to accommodate various-sized samples. For the transfer mechanism, a simple tongue-in-groove assembly, moved between chambers by means of a transfer arm which would screw into the side of the susceptor, was deemed simplest and most practical.

E. Conclusions

A design to deposit SiC thin films has been developed. Various components have been designed and either received or assembled and others are being ordered at this time. Other needed parts are currently being machined.

F. Future Research Plans and Goals

Further assembly of the system is expected as parts become available upon receipt or after fabrication.

III. *Ex Situ* and *In Situ* Methods for Complete Oxygen and Non-Carbidic Carbon Removal from $(0001)_{Si}$ 6H-SiC Surfaces

A. Introduction

For SiC to succeed as the substrate/semiconductor of choice for high-frequency, high-temperature, high-power devices and III-N heteroepitaxy, a considerable reduction in defects (line, planar, point, etc.) must be achieved. Following Si technology, where surface cleaning and preparation are critical first step in all processes [1], a continued reduction in defects in SiC should be expected as a result of improved SiC wafer surface cleaning techniques. In Si technology for example, improper removal of surface contamination and oxides prior to Si homoepitaxy has been shown to result in an increase in the density of line and planar defects in epitaxial films from $< 10^4/cm^2$ to $> 10^{10}/cm^2$ [2-5] and an associated drop in device yield [2].

Typically, SiC *ex situ* cleaning consists of solvent degreasing and RCA cleaning with the last step usually a 5-10 min. dip in an HF solution (composition ranging from 0.1-50%) [6-8]. The HF dip is intended to remove any native or intentionally grown (dry or thermal) oxides formed on the SiC surface. For silicon, the HF etch has been found to be beneficial in that it not only removes oxides (SiO_2 or SiO_x) from the surface but also passivates the surface by terminating all the dangling bonds with hydrogen [9-11]. The hydrogen termination inhibits re-oxidation of the silicon surface on removal from the HF solution and produces a hydrophobic surface [11]. For $(0001)_{Si}$ 6H-SiC, this has not been found to be the case. Surface analysis by the authors and others (see Fig. 1a) has revealed that the SiC surface is still terminated with an $\approx$ 10 Å layer of carbonaceous material (consisting or C-C, C-O, C=O, and C-H bonding) after HF dipping [7-9]. Thermal desorption of this non-carbidic carbon can be easily achieved by annealing at temperatures as low as 500-700°C. However, unlike Si, approximately 1/2 to 3/4 monolayer of oxide remains at the surface (see Fig. 2a-b), and thermal desorption of this oxide in UHV requires temperatures in excess of 1000°C [12]. In Fig. 1c, removal of the oxide by this method can result in the formation of some non-carbidic/graphitic carbon at the SiC surface. To combat this, others have followed the pioneering work of Kaplan [13] and employed *in situ* techniques in which the SiC surface is annealed in a flux of Si (solid or gas source) which allows thermal desorption of the oxide at lower temperatures (< 900°C) while maintaining a Si-rich surface [12,14]. This section reports efforts to use a Si capping layer to provide both a hydrophobic surface during *ex situ* processing and a Si-rich surface during *in situ* processing.

B. Experimental

The vicinal n-type (typically $N_d = 10^{18}/cm^3$) $(0001)_{Si}$ 6H-SiC wafers used in these experiments contained an n type epilayer (typically $N_d = 10^{17}/cm^3$) and 500-1000Å of thermally

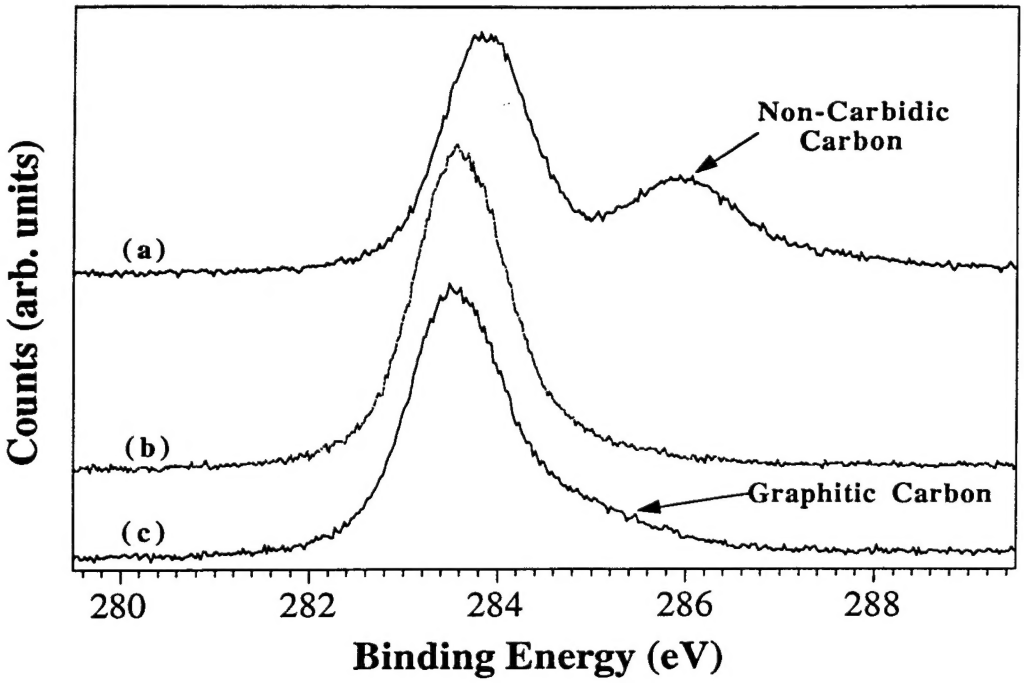

Figure 1. XPS of C 1s from $(0001)_{Si}$ 6H-SiC surface after: (a) 5 min. 10:1 HF dip, (b) after thermal annealing at 800°C, and (c) after annealing at 1200°C in UHV [8].

grown oxide. They were supplied by Cree Research, Inc. The thermal oxide was removed using a 5-10 min. dip in a 10:1 HF dip (CMOS grade, J. T. Baker). Further cleaning of this surface was then investigated by immersion in other acid/base solutions or by reoxidizing the SiC surface using a UV/O_3 treatment followed by a wet chemical treatment. The UV/O_3 treatments described in this study employed a box in which was positioned a high intensity Hg lamp in close proximity to the SiC wafer. The details of this process have been described previously [15]. The wet chemistries examined included 10:1 HF, 10:1 buffered HF (7:1 NH_4F:HF), 40% NH_4F, HCl:HF, and NH_3OH:HF solutions, HNO_3, H_2SO_4, acetic, and lactic acid. Except where noted, after all wet chemical cleans the samples were rinsed in DI water (18 MΩ) and blown dry with N_2 (UHP). All wet chemicals were of CMOS grade purity (J. T. Baker).

The *in situ* cleaning and the surface analyses of the samples subjected to *ex situ* and *in situ* cleaning were conducted in a unique ultra-high vacuum (UHV) system consisting of a 36 ft. long UHV transfer line to which were connected several surface analysis and thin film deposition units. The details of each and the transfer line have been described elsewhere [15]. Surfaces prepared in the above manner were then subsequently mounted to a molybdenum sample holder and loaded into the loadlock for subsequent analysis by AES, XPS, EELS, and LEED. XPS analysis was performed using the Al anode ($h\upsilon$ = 1486.6 eV) at 20 mA and 10kV. AES spectra were obtained using a beam voltage of 3 keV and an emission current of

1 mA. LEED was performed using rear view optics, a beam voltage of approximately 100 eV, and an emission current of 1 mA. Calibration of the XPS binding energy scale was performed by measuring the position of the Au $4f_{7/2}$ and shifting the spectra such that the peak position occurred at 83.98 eV. All sample temperatures quoted here were measured using an optical pyrometer and an emissivity of 0.5.

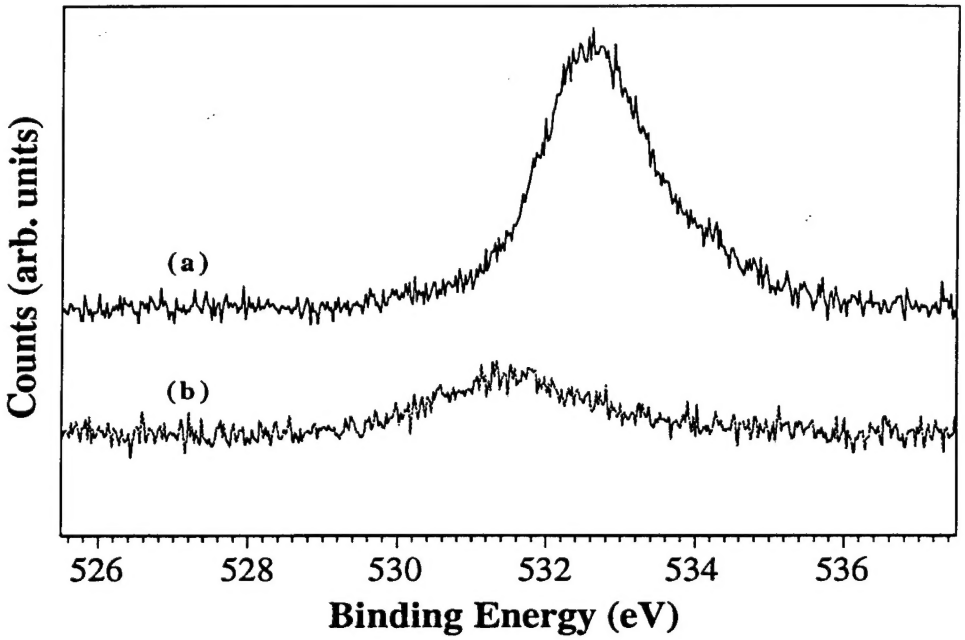

Figure 2. XPS of O 1s from (a) $(0001)_{Si}$ 6H-SiC and (b) Si (111) wafers after dipping in 10:1 HF for 5 min [12].

C. Results

Si and SiC Wetting Experiments. As previously mentioned, oxide removal from (0001) 6H-SiC surfaces using HF leaves a hydrophilic surface containing significant amounts of oxide surface (see Fig. 3a). To determine a wet chemistry which produces a more hydrophobic SiC surface, several $(0001)_{Si}$ 6H-SiC wafers were dipped in HF, NH_4F, NH_3OH, HCl, HNO_3, H_2O_2, H_2SO_4, acetic acid, and lactic acid and the wetting characteristics of these surfaces in these acids and bases and de-ionized water monitored visually. For comparison purposes, Si (111) and Si (100) wafers were also dipped simultaneously in each acid with the SiC wafer. All wafers (Si or SiC) were initially dipped in 10% HF to remove any native oxides from the surfaces before dipping in the acids and bases of interest. For Si, the surfaces remained hydrophobic when dipped in NH_3OH, HCl, or H_2O_2. Dipping the Si wafers in HNO_3 or H_2SO_4 removed the hydrophobic nature of the surface. Dipping Si in the organic acids resulted in a strongly adhering thin film of the acid to the silicon surface which could be removed in DI H_2O leaving a hydrophobic surface. For SiC, all acids and bases wetted the surface and none

were found to produce a hydrophobic SiC surface. 10% HF solutions with pH's adjusted from strongly acidic, neutral, and to strongly basic using HCl, NH_4F, and NH_3OH, respectively, were also examined as they have been reported to produce better hydrogen termination of Si (111) surfaces [17,18]. In these experiments, the dipping times were held constant at 10 min. No changes in the wetting characteristics of the $(0001)_{Si}$ SiC surface in HF solutions with the different pH's were found. In an additional experiment, the dipping time was varied from 5 min. to 1 hr.; however, no difference was found. Additionally, neither XPS nor AES indicated a significant change (within AES and XPS experimental accuracy) in the amount of surface oxygen on $(0001)_{Si}$ SiC wafers after dipping in HF solutions of various pH. No differences were observed between on axis and vicinal surfaces, as well.

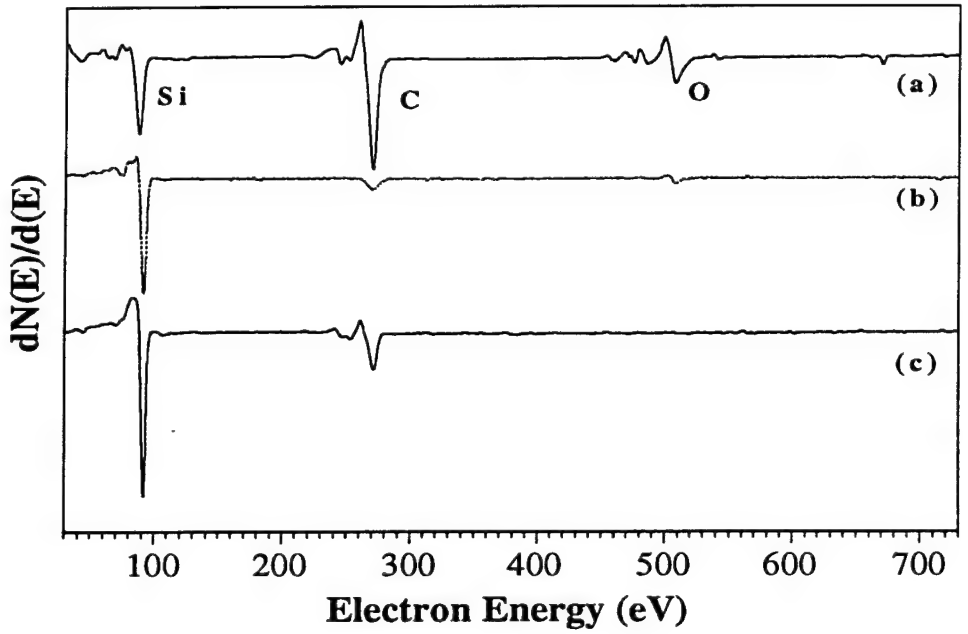

Figure 3. (a) AES of (0001)Si 6H-SiC surface after dipping in 10:1 HF for 5 min., (b) $(0001)_{Si}$ 6H-SiC with a 20Å Si capping layer after dipping in 10:1 HF, 5 min., (c) $(0001)_{Si}$ 6H-SiC after hermal desorption of the Si capping layer at 1100°C for 5 min.

Si Capping Layer. A new technique for *in situ* oxide removal rapidly gaining acceptance consists of annealing SiC in a flux of silicon at temperatures > 900°C [13,14]. Since wet chemical cleaning of Si was found to more readily produce hydrophobic and cleaner surfaces, the use of a 20Å Si capping layer on $(0001)_{Si}$ 6H-SiC was investigated. The following procedure was used to prepare the Si capping layer. Firstly, the (0001) 6H-SiC wafer was given a 5 min. dip in 10:1 HF, DI rinsed, N_2 blow dried and loaded into vacuum. The 6H-SiC was then degassed and annealed in a SiH_4 flux (10^{-6} Torr) at 950°C for 20 min. in the

GSMBE. This produced an oxygen free Si rich (1×1) SiC surface. Next, a Si-Ge electron beam MBE was used to deposit 200Å of Si on the SiC at room temperature *in situ*. The Si/SiC sample was then given two UV/O_3 treatments followed by dips in 10:1 HF to thin the Si capping layer down to 20Å. After each HF dip, the polished face of the Si/SiC wafer was found to be hydrophobic as with Si wafers. AES of this surface after HF dipping showed only small amounts of oxygen and carbon contamination (see Fig. 3b). XPS of this surface after HF exposure showed a Si 2p peak at 99.5 eV with a shoulder at 101.5 eV indicating that the surface consisted of an ≈ 20 Å Si film on top of the SiC. On annealing this surface to desorb the Si capping layer, it was observed that the outgassing from the wafer was several orders of magnitude lower than that typical for other HF dipped SiC wafers (10^{-7} Torr ax vs. 10^{-5} Torr typical). In fact, the outgassing levels were typical for those observed from Si (111) wafers. The reason's for these higher and lower outgassing rates will be discussed later.

Following annealing of the Si/SiC wafer at 1100°C for 5 min., LEED showed a sharp (3×3) reconstructed surface commonly observed for surfaces prepared via annealing in Si fluxes [12]. XPS of this surface, now shows a Si 2p peak located at 101.5 eV with a shoulder at 99.5 eV indicating that the 3×3 surface is due to the presence of a Si bilayer. Continued annealing at 1100°C resulted in further desorption of Si which resulted in first a (1×1) and then a ($\sqrt{3}$x$\sqrt{3}$)R30° LEED pattern. AES of the (3×3) surface showed no oxygen within the detection limits of AES and a Si/C ratio of 3/1. It should be pointed out that (3×3) surfaces

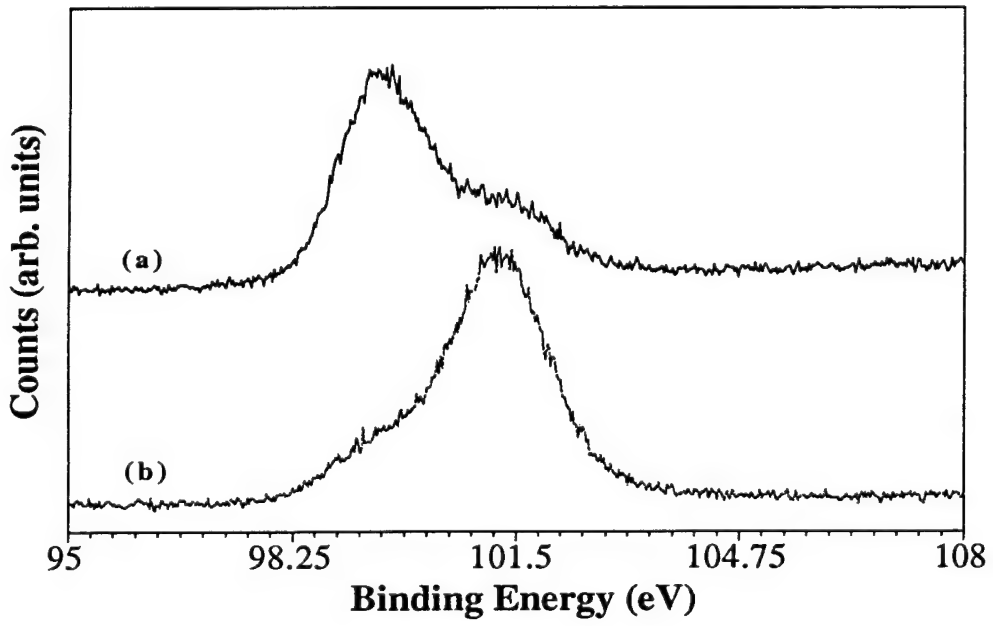

Figure 4. XPS of Si 2p from a $(0001)_{Si}$ 6H-SiC with a 20Å Si capping layer after: (a) 5 min. dip in 10:1 HF, and (b) after thermal desorption of the Si capping layer at 1100°C for 5 min.

have been previously prepared, removed from vacuum, dipped in HF, and the wetting characteristics observed. In this case, the surfaces were hydrophilic indicating that the Si bilayer is readily removed by the combination of air exposure and HF dipping. As such, 15-20 Å probably represents the optimum thickness for the Si capping layer.

D. Discussion

One frequently noted problem with (0001) 6H-SiC wafers is the existence of internal micro-pipes. Aside from being potential device killers, the authors have frequently experienced other problems during processing of SiC wafers which can be attributed to the micro-pipes as well. The authors have frequently observed that these entities can harbor HF and H_2O after HF dipping and N_2 drying. Presumably, this is due to capillary action. This conclusion is based primarily on the observation that during annealing/thermal desorption in UHV of HF dipped SiC wafers phenomenally high outgassing rates have been observed (i.e. 10^{-5} Torr). RGA analysis of the background vacuum during thermal annealing of the SiC wafer reveals that HF and H_2O are the two main constituents outgassing from the wafers. As outgassing rates for Si wafers which have experienced an HF dip & N_2 dry are several orders of magnitude lower (10^{-8} to 10^{-7} Torr), we suggest that HF/H_2O trapped in the micro-pipes due to capillary action are the source of the extremely high outgassing. The importance of this observation is that the high outgassing can lead to difficulties in completely removing the oxide from the SiC surface as well as creating a large background of H_2O and HF in the growth system. The H_2O/HF levels can subsequently result in an increase of background oxygen or fluorine in epitaxial films. Owing to the observed change from a hydrophilic to a hydrophobic surface with the addition of the Si capping layer, it is not surprising that lower outgassing rates were observed for the SiC surface with the Si capping layer.

In addition to the oxide removal and the lower outgassing rates, another advantage of the use of the Si capping layer is the potential for its incorporation into already existing processing routes. Potentially, the Si capping layer could be deposited during cooling from SiC thin film CVD epitaxy. Currently, the SiC wafer/film assemblies are cooled in H_2 which produces a carbon rich layer which must be removed by a second processing step of thermal oxidation [9,18]. Unfortunately, high quality SiC CVD epitaxial deposition typically occurs at temperatures higher than the Si melting point (1440°C) and hence results in the deposition of Si droplets instead of a continuous film of Si [19]. However, the authors have initially found that this approach can still eliminate the need for oxidation as the Si droplets can be etched away (15 HNO_3: 2 HF: 5 CH_3COOH) leaving a surface concentration equal (by XPS and AES) to that produced by thermal oxidation and oxide removal by HF. Perhaps, the Si capping layer can best be utilized with 3C-SiC surfaces where epitaxy can occur at lower temperatures.

E. Conclusions

The wetting characteristics of (0001) 6H-SiC surfaces in HF and other acids were found to be hydrophilic. Hydrophobic surfaces could be achieved by use of a thin 20 Å Si capping layer. The use of the capping layer also resulted in lower outgassing rates during thermal annealing during *in situ* processing. Annealing the Si capping layer/SiC wafer at 1100°C for 5 min. resulted in the desorbtion of the excess silicon and a (3×3) reconstructed SiC surface.

F. Acknowledgments

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IV. Rectifying and Ohmic Contacts for P-type Alpha (6H) Silicon Carbide

A. Introduction

While the wide band gap of SiC is responsible for its use in optoelectronic, high power, and high temperature devices, this property also adds to the difficulty of controlling the electrical properties at the metal-semiconductor contacts in these devices. The primary parameter used to quantify the electrical relationship at these interfaces is the Schottky barrier height (SBH), or the energy barrier for electrons traversing the interface. A small SBH is desired for a good ohmic, while a relatively large SBH is necessary to create a good rectifying contact.

The formation of low resistivity and thermally stable ohmic contacts to 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have the advantage over Si, the contact resistivities must be below 1×10^{-5} Ω-cm^2 [1]. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally contained Al to dope the SiC surface below the contacts. While the fabrication of ohmic contacts to SiC also has usually depended on very heavily-doped surfaces, the introduction of high levels of dopants in the near surface device region of the epilayer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice. Based on all of these issues and experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

Low resistance contacts to p-type SiC remain a substantial challenge for high temperature and high-power devices. An Al-Ti alloy [2] annealed at 1000°C for 5 min. was reported to yield contact resistances ranging from 2.9×10^{-2} Ω cm^2 for a carrier concentration of 5×10^{15} cm^{-3} to 1.5×10^{-5} Ω cm^2 for 2×10^{19} cm^{-3}. The thermal stability of these contacts was not reported. Aluminum deposited on a heavily-doped 3C-SiC interlayer on a 6H-SiC substrate and subsequently annealed at 950°C for 2 min. reportedly yielded contact resistivities of $2\text{–}3\times10^{-5}$ Ω cm^2 [3]. Because of its low melting point (660°C), however, pure Al would be unsuitable for high temperature applications. Platinum contacts annealed from 450 to 750°C in 100°C increments were also used as ohmic contacts to p-type SiC [4]. These contacts, which rely on the combination of a highly-doped surface and the high work function of Pt, have not been known to yield contact resistivities as low as those for contacts containing Al.

B. Experimental Procedure

Vicinal, single-crystal 6H-SiC (0001) wafers provided by Cree Research, Inc. were used as substrates in the present research. The wafers were doped with N or Al during growth to

create n- or p-type material, respectively, with carrier concentrations of $1–5\times10^{18}$ cm^{-3}. Homoepitaxial layers (1–5 μm thick) grown by chemical vapor deposition (CVD) were Al-doped with carrier concentrations ranging from 1×10^{16} to 1×10^{19} cm^{-3}. The surfaces were oxidized to a thickness of 500–1000 Å in dry oxygen. The substrates were cleaned using a 10 min. dip in 10% hydrofluoric acid, transferred into the vacuum system, and heated at 700°C for 15 min. to remove any residual hydrocarbon contamination.

A UHV electron beam evaporation system was used to deposit the NiAl, Ni, Au, Pt, and Cr-B films. After depositing 1000 Å of NiAl, 500–1000 Å of Ni was deposited as a passivating layer. Pure Ni (99.99%) and pure Al (99.999%) pellets were arc melted to form alloyed pellets of 50:50 atomic concentration for evaporation of NiAl. The films were deposited onto unheated substrates at a rate of 10–20 Å/s. Chromium and B were evaporated simultaneously from separate evaporation sources. The pressure during the depositions was between 5×10^{-9} and 5×10^{-8} Torr.

Circular contacts of 500 μm diameter were fabricated for electrical characterization by depositing the metal films through a Mo mask in contact with the substrate. Silver paste served as the large area back contact. For contact resistance measurements, TLM patterns [5] were fabricated by photolithography. The Ni/NiAl films were etched in phosphoric acid : acetic acid : nitric acid (12 : 2 : 3) at 50°C (etch rate ≈ 30 Å/s). The contact pads were 300×60 μm with spacings of 5, 10, 20, 30 and 50 μm. Mesas in the substrate were not fabricated. All annealing was conducted in a N_2 ambient in a rapid annealing furnace.

Electrical characteristics were obtained from current-voltage and capacitance-voltage measurements. Current-voltage (I-V) measurements were obtained with a Rucker & Kolls Model 260 probe station in tandem with an HP 4145A Semiconductor Parameter Analyzer. Capacitance-voltage (C-V) measurements were taken with a Keithley 590 CV Analyzer using a measurement frequency of 1 MHz.

Auger electron spectroscopy (AES) was performed with a JEOL JAMP-30 scanning Auger microprobe. The films were sputtered with Ar ions at a beam current and voltage of 0.3 μA and 3 kV, respectively, to obtain composition profiles through the thickness of the films.

C. Results and Discussion

Chemical Characterization of As-deposited Films. An Auger depth profile of a film deposited from the NiAl source showed that the overall composition remained relatively stable. The relative compositions of Ni and Al were calculated by referencing to pure Ni and pure Al standards and accounting for their corresponding sensitivity factors. The average atomic composition was approximately 50:50. With reference to Cr and B standards, the Cr-B film was determined to be comprised of approximately 20% Cr and 80% B (CrB_4). While a thin

oxide layer was detected at the surface of the NiAl film, no O was detected within either of the films.

Schottky Contacts. In the as-deposited condition the Ni/NiAl contacts were rectifying on p-type SiC with carrier concentrations of 1.6×10^{16} and 3.8×10^{18} cm^{-3} in the epilayer. The sample with the lower carrier concentration displayed leakage current densities of $\sim1\times10^{-8}$ A/cm^2 at 10 V and ideality factors between 1.4 and 2.4, while the latter sample displayed approximately five orders of magnitude higher leakage current densities and similar ideality factors. The average Schottky barrier heights (SBH's) calculated for the samples with the lower and higher carrier concentrations were 1.37 and 1.26 eV, respectively. The lower SBH calculated for the former sample is likely due to enhanced thermionic field emission through the upper energy region of the barrier because of the narrower depletion region. Hence, the 1.37 eV value is believed to be more accurate.

Similar results were obtained for as-deposited Ni, Au, and Pt contacts on p-type ($2.1–4.5\times10^{16}$ cm^{-3}) 6H-SiC (0001). These samples displayed similar leakage currents and ideality factors of 1.3–2.1 and <1.1, respectively. From these measurements SBH's of 1.31 eV for the Ni contacts and 1.27 eV for the Au contacts were calculated. In comparison, as-deposited Ni on n-type (4.1×10^{16} cm^{-3}) 6H-SiC (0001) yielded ideality factors below 1.1, similar leakage current densities to those stated above, and SBH's of 1.14 eV and 1.21 eV calculated from I-V and C-V measurements, respectively.

Our measurements on p-type SiC have shown consistent differences from measurements on n-type 6H-SiC. The SBH's tended to be higher on p-type than on n-type material. While leakage currents for Au, NiAl, and Ni contacts on p-type 6H-SiC were comparable to Ni contacts on n-type 6H-SiC, the ideality factors were higher on p-type SiC. These ideality factors and SBH's are higher than for Ni contacts (and other previously studied contacts) on n-type 6H-SiC (0001). The higher ideality factors indicates that thermionic emission was not the dominant current transport mechanism in the p-type SiC and may indicate the occurrence of recombination at deep levels.

On the other hand, the relationship between the SBH's of the metals on p-type SiC and their respective work functions was similar to that which we previously found for n-type SiC. The calculated SBH's on p-type SiC are plotted vs. the metal work functions in Fig. 1. The work function for NiAl was taken to be the average of the work functions for pure Ni and pure Al since a value was not found in the literature for NiAl. The slope of the line fit to the empirical data was -0.28 as compared to a slope of -1.0 for the theoretical data. These results indicate that surface states on p-type 6H-SiC (0001) cause a partial pinning of the Fermi level, in agreement with the results of our previous, extensive study on n-type SiC.

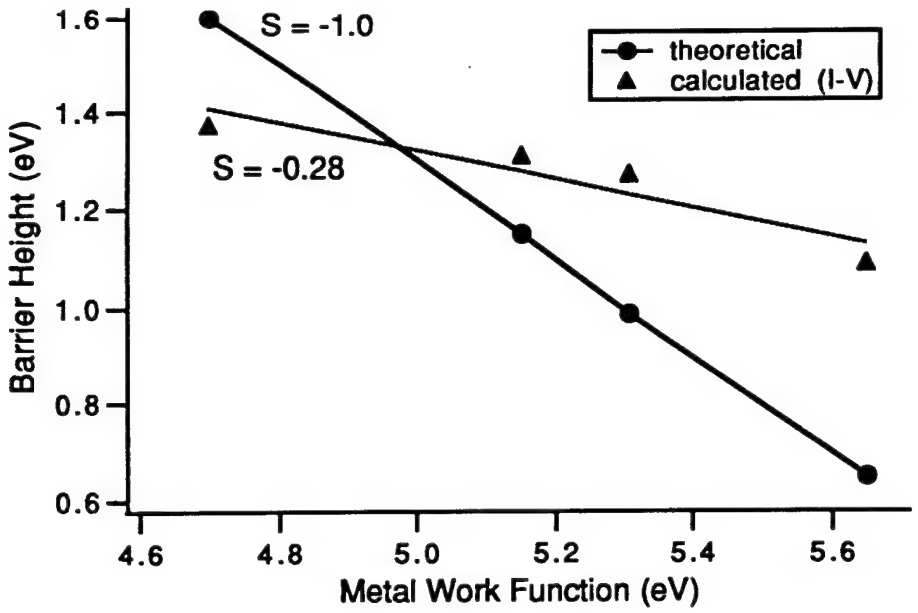

Figure 1. Graph of calculated and theoretical barrier heights of as-deposited NiAl, Au, Ni, and Pt contacts on p-type 6H-SiC vs. metal work function. The calculated values were determined from I-V measurements, and the theoretical values were calculated according to the Schottky-Mott limit. The slopes, S, of the lines fit to each set of data are indicated on the graph.

Ohmic Contacts. The Ni/NiAl contacts were sequentially annealed for total times of 10–80 s at 1000 °C in a N_2 ambient. This temperature was used because (1) limited intermixing of Al and SiC was reported at 900°C [6] and (2) other papers report annealing in this temperature range for Al-based ohmic contacts on p-type SiC [2,3,7]. Because of the extremely high thermodynamic driving force for Al to form an insulating oxide layer (ΔG_f (Al_2O_3) ~ -1300 kJ/mol at 1000 °C [JANAF - Chase, M., et al., JANAF Thermochem. Tables, 3d Ed. J. Phys. Chem. Ref. Data, 1985. 14(Supp. 1)]), 1000 Å of Ni was deposited on top of the NiAl contacts to slow the oxidation process.

Table I summarizes the results of I-V measurements taken at selected intervals through the annealing series for three samples with various carrier concentrations in the SiC epitaxial layer (1.4×10^{18}, 5.7×10^{18}, and 1.5×10^{19} cm^{-3}). The two samples with the lower carrier concentrations were not truly ohmic but became ohmic-like after annealing for 80 s. The additional force on the probes needed to obtain consistent results indicates that an oxide began to form at the surface which would likely cause more severe problems if the samples were annealed further. The sample with the higher carrier concentration was ohmic after annealing for 10 s. The calculated specific contact resistivity remained approximately 2.0×10^{-2} Ω cm^2 through annealing for 60 s. A slight increase to 3.1×10^{-2} Ω cm^2 was calculated after annealing for 80 s. This increase is believed to be due to the surface oxide layer.

Table I. Estimated specific contact resistivities / electrical behavior of Ni (1000 Å) / NiAl (1000 Å) / p-SiC after annealing at 1000 °C for 20, 40, 60, and 80 s for three samples with the carrier concentrations indicated. The specific contact resistivities were calculated from non-mesa etched linear TLM patterns.

Annealing Time	20 s	40 s	60 s	80 s
1.4×10^{18} cm^{-3}	non-ohmic	non-ohmic	non-ohmic	almost ohmic
5.7×10^{18} cm^{-3}	non-ohmic	non-ohmic	non-ohmic	almost ohmic
1.5×10^{19} cm^{-3}	2.0×10^{-2} Ω cm^2	1.9×10^{-2} Ω cm^2	2.2×10^{-2} Ω cm^2	3.1×10^{-2} Ω cm^2

An Auger depth profile (Fig. 2b) of Ni/NiAl/SiC annealed at 1000°C for 80 s shows that the surface oxide is thicker than that on the as-deposited sample (Fig. 2a). After sputtering for a couple of minutes, the O concentration dropped to below detectable limits; however, the data shows a decreasing Al concentration in the direction toward the SiC interface. This indicates that the kinetics are more favorable for the Al to diffuse toward the surface and react with O than for the Al to react with the SiC. Some of the Ni has probably reacted with Si at the interface to form a silicide, as indicated by the local maximum in the Ni intensity near the SiC interface, while the peak in the C intensity indicates the presence of an adjacent C-rich layer.

The demonstrated oxidation problem with Al necessitates the development of ohmic contacts which do not consist of substantial concentrations of Al. To reduce this problem we have chosen to investigate contacts which contain B.

The main reasons for choosing B are that it is also a p-type dopant in SiC, its oxide is not as stable, and it is a much faster diffusant in SiC. Table II compares some important properties of B, Al, and their associated oxides. Recent reports [8,9] show that the 'shallow' activation energy for B in SiC is significantly less than previously reported. Boron compounds tend to be more stable at high temperatures than aluminum compounds which suffer from the low melting point of Al. Also, the diffusion coefficient of B is at least three orders of magnitude greater than that of Al. Therefore, more B than Al will diffuse into the SiC at lower temperatures. As discussed in this report, a major problem with Al-based contacts is the strong driving force for forming an insulating oxide layer. This situation is shown by the extremely low equilibrium partial pressure, p_{O_2}, for Al_2O_3 formation. While B_2O_3 also has a low p_{O_2}, it is significantly higher than that for Al_2O_3, indicating that the driving force for B to form an oxide is significantly lower. There is also a larger number of metals which would reduce the oxide formed with B than that formed with Al, a fact which is encouraging when one is trying to diffuse free B into SiC. Another advantage is that the melting point of boron oxide is notably low.

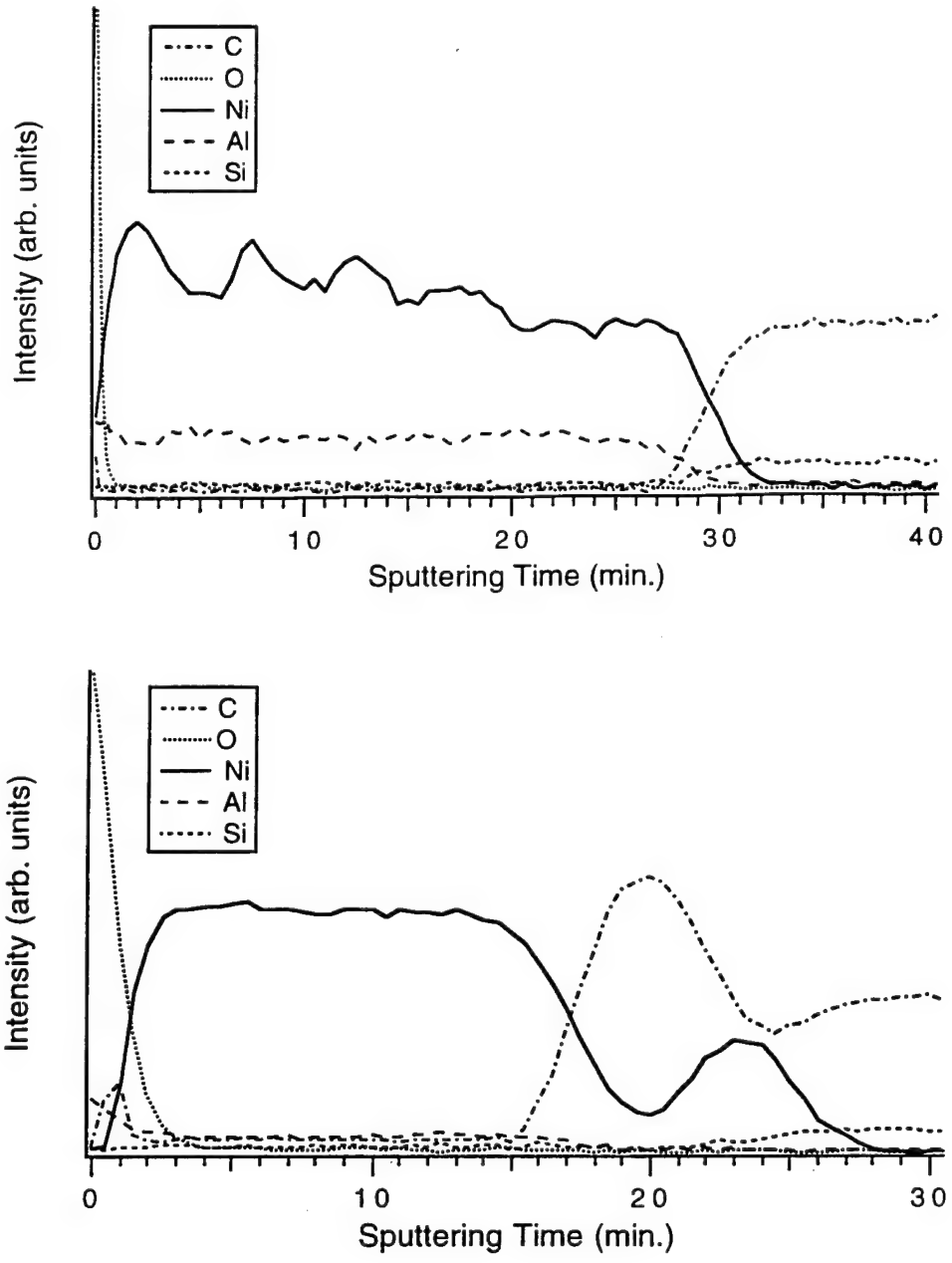

Figure 2. AES composition profile of (a) NiAl (1000 Å) deposited at room temperature on (0001) 6H-SiC and (b) Ni (1000 Å) / NiAl (1000 Å) / 6H-SiC annealed at 1000 °C for 80 s in N_2.

Several boron compounds which possess reasonably low resistivities and high melting temperatures are listed in Table III. We have chosen to investigate Cr-B contacts because of the relative ease to deposit these materials by electron beam evaporation and the demonstrated use of Cr in metallization schemes for diffusion barriers. The refractory nature of these materials increases the probability of forming ohmic contacts which will be stable at high temperatures.

Table II. Selected Properties of B, Al, and Their Associated Oxides

Element	Activation Energy in 6H-SiC (meV)	Solid Source Diffusion, D_{SiC} @ 1800°C (cm^2/s)	Equilibrium partial pressure of O_2, p_{O_2} @ 700°C (torr)	Melting temp. of the associated oxide, T_{melt} (°C)
B	700	10^{-11} [10-11]	10^{-35}	450
Al	240	$<10^{-14}$ [12]	10^{-47}	2040

Table III. Resistivities and Melting Points of Selected Boron Compounds

Compound	Electrical Resistivity (μΩ-cm) 298 K [13]	Melting Temperature (°C) [14]
CrB_2	30	2200
GdB_4	31	2650
MoB	45	2600
NbB_2	26	3000
TaB_2	33	3037
VB_2	23	2747
ZrB_2	10	2972

Cr and B were simultaneously deposited on p-type 6H-SiC epitaxial layers, some of which had not been oxidized to prevent the reduction of the Al dopant near the surface during oxidation. The carrier concentrations in the epitaxial layers ranged from 1×10^{18} to 8×10^{18} cm^{-3}. The as-deposited contacts for the sample with a carrier concentration of 1×10^{18} cm^{-3} displayed rectifying behavior with low leakage currents (~4×10^{-8} at 10 V) and ideality factors between 1.5 and 1.9. Rectification was expected since the contacts had not been annealed, and large SBH's normally exist for as-deposited contacts on p-type SiC.

The samples were annealed at 1000°C for total times varying from 60 to 300 s in an Ar ambient. A subsequent anneal for 60 s at 1100°C in Ar was also performed. After 60 s at 1000°C, the contacts showed substantial changes in their electrical characteristics. The contacts became very leaky, or semi-ohmic. As the annealing time increased, the contacts became more ohmic-like and the resistivity decreased. A slight increase in resistivity of many of the contacts was displayed after annealing at 1100°C. An insulating oxide at the surface, which was a problem after annealing Ni/NiAl/SiC at 1000°C for 60-80 s, has not been a problem during electrical probing of the annealed Cr-B contacts.

D. Conclusions

Nickel-aluminum was investigated primarily as an ohmic contact for p-type 6H-SiC because of the p-type doping of Al in SiC, the high melting point of NiAl (as compared to Al), and the tendency of Ni to form silicides but not carbides. This latter property potentially could have resulted in extraction of Si from the SiC lattice in exchange for Al, thereby enhancing the p-type carrier concentration at the surface. Although the I-V measurements indicate that some Al may be diffusing into the SiC after the longest annealing time performed (80 s at 1000°C), this potential for reaction between Al and SiC appears to be exceeded by the driving force for Al to diffuse to the surface and react with O. A concentration profile obtained from AES analysis shows that Al has diffused through the 1000 Å Ni overlayer to form a thin (200 Å estimated) oxide layer.

In addition to the ohmic behavior resulting from annealing the NiAl contacts, as-deposited Ni, NiAl, and Au contacts deposited at room temperature on p-type ($N_A < 5\times10^{16}$ cm^{-3}) 6H-SiC (0001) were rectifying with low leakage currents, ideality factors between 1.3 and 2.4, and SBH's of 1.31, 1.27, and 1.37 eV, respectively. These results indicate that the Fermi level is partially pinned at p-type SiC surface, in agreement with our previous results on n-type SiC.

As an alternative to Al for fabricating ohmic contacts to p-type 6H-SiC, Cr-B contacts were investigated because of its low resistivity, high melting temperature, and reduced tendency for oxidation of B (compared to that of Al). In the as-deposited condition these contacts were rectifying with low leakage currents. After annealing at 1000 °C for 60 s, the contacts displayed semi-ohmic behavior and became less resistive with successive 60 s anneals to a total time of 300 s. This annealing series will be continued.

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V. Development of a System for Integrated Surface Cleaning and Oxide Formation on 6H-SiC

A. Introduction

The development of high-temperature, -power and -frequency devices based on SiC requires a more complete understanding of the oxide formation and interface characteristics. By using an integrated UHV system, interfaces will be prepared with lower contaminant levels while gaining a better understanding of the SiC oxide formation process. Current difficulties of oxide formation on p-type SiC will be investigated. By maintaining the flexibility of the system, it can be adapted to produce the most promising results. The UHV compatible surface preparation and oxide formation system will be integrated with an advanced system that includes other processing and characterization capabilities that will allow for *in vacuo* characterization of the SiO_2/SiC interface and oxides grown by various individual and combination processes. These oxides will be tested for their electrical characteristic for device applications.

B. Experimental Procedure

The integrated system will allow for most of the characterization to be accomplished without exposing samples to the ambient. Furthermore, the processes will be characterized at various stages in the process, thus, allowing for the understanding of the entire oxidation process. A typical process is given as follows: (1) surface preparation; (2) initial insulator formation; (3) CVD insulator deposition. A schematic of the process is shown in Fig. 1. At each of these stages, a wide variety techniques are available.

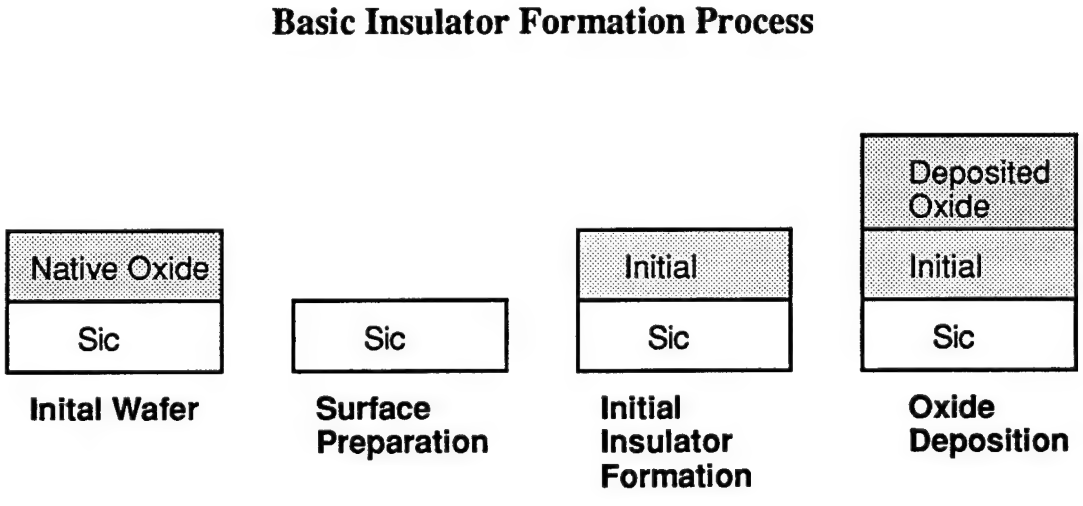

Figure 1. Basic process for insulator formation on SiC.

Surface preparation is arguably the most important step to high-quality insulator growth. Ensuring a clean smooth surface for oxide growth will allow for the examination of the SiC/SiO_2 interface with little concern for surface contamination and roughness. Some of the various procedures are: (1) wet chemical clean ; (2) plasma cleaning; (3) HF vapor phase. By using these procedures and combinations thereof, it is planned to develop an excellent process for the surface preparation on SiC.

Initial insulator formation on SiC is where the current problem with lies. On p-type SiC there is considerable dopant redistribution and defect formation during the transition region between SiC/SiO_2. By using diverse techniques for initial insulator formation, observations will be made of which process or combination of processes will minimize defect formation, dopant redistribution, and maximize the electrical properties on the initial oxide formation. Some of the procedures are: (1) UV ozone; (2) Nitric bath; (3) plasma enhanced CVD (PECVD).

CVD insulator formation is the final step in the oxide formation process. Here, oxide is deposited on the initial oxide to the desired thickness. This process is well understood and is believed to pose little difficulty. Electrical characteristics are then determined. C-V and I-V measurements will be made to determine defects, such as trapped charge and interface charge.

An unique capability that will be employed in this study is the processing system integrated with *in vacuo* diagnostics. The system which is shown schematically in Fig. 2, includes

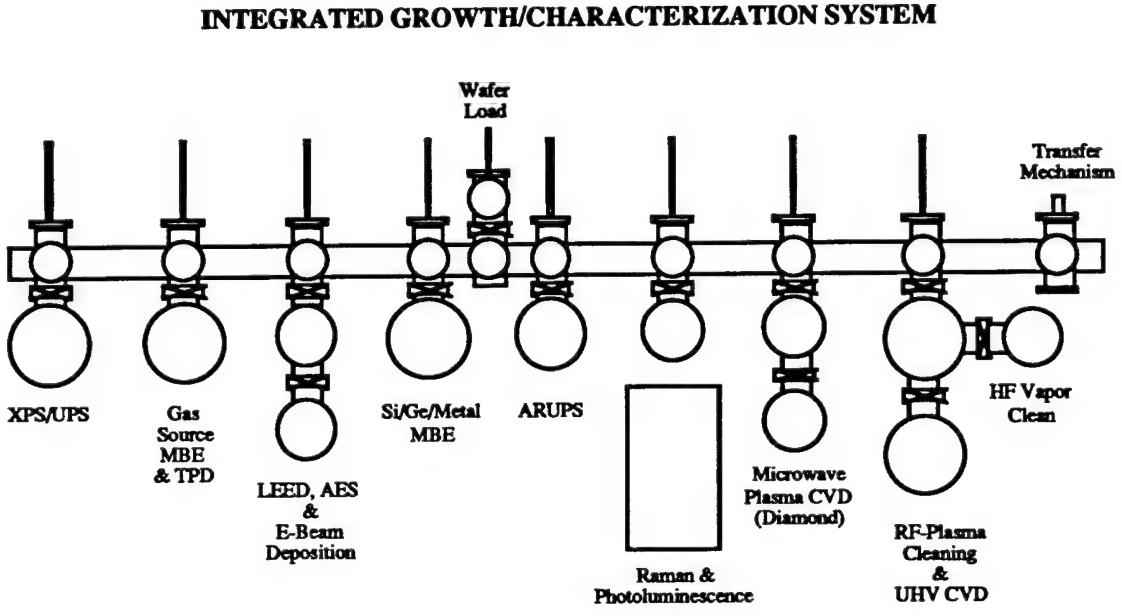

Figure 2. Schematic of the integrated growth and characterization system to be employed in the studies of defects in insulators on SiC.

advanced surface characterization, surface preparation, and growth capabilities. Included in this project is the development of a UHV CVD/oxidation system which would be constructed to be compatible with the integrated system. The system is based on a UHV linear sample transfer mechanism. This transfer chamber which is 40 ft. long, connects eight separate surface preparation, processing or characterization chambers. Techniques relevant to this study include the remote plasma surface preparation chamber, LEED, AES, XPS, UV-photoemission, thermal desorption, and AlN deposition. Other chambers which could prove useful include *in situ* Raman spectroscopy, field emission, and Si MBE.

C. Conclusions

The integrated UHV system will be able to explore processes that have previously been unobtainable. The uniqueness of the surface preparation integrated with the growth and characterization system allows for capabilities that have not been previously used in the characterization and growth of oxides on SiC. The electrical characteristics will drive the thrust of the research areas.

D. Future Research Plans and Goals

There will be considerable focus on the examination of the oxide layers for use as gate insulators in field effect devices. A process by which the gate oxide and gate can be applied to an industrial setting will be attempted.

VI. Characterization of Oxides on N- and P-Type 4H- and 6H-SiC

A. Introduction

Silicon carbide (SiC) has been shown to be an excellent material for the fabrication of devices for high power, high frequency and high temperature applications [1]. The advantages of SiC metal oxide semiconductor field effect transistors (MOSFETs) has also been discussed [2]. The successful operation of these devices hinges on the interface and bulk properties of the gate dielectric, usually an oxide. Previous researchers have reported results on thermally grown oxides on N-type [3-6] and P-type 6H-SiC [5,7-11]. While the results obtained on N-type 6H-SiC have shown that those oxides are of high quality, oxides grown on P-type 6H-SiC exhibit large flatband voltage shifts and are, thus, unsatisfactory for application as gate dielectrics. Oxides deposited under special conditions with surface preparation specific to the particular deposition might show improved interfacial properties over thermally grown oxides.

The SiO_2-SiC interfaces will be characterized using capacitance-voltage (C-V) measurements [12]. A Mask set has been designed to fabricate the MOS structures required for accurate and complete electrical characterization. The Mask set, fabricated at DuPont Photomasks Inc. has been delivered, as well as the SiC wafers required for processing. Device processing was commenced this quarter.

B. Experimental Procedure

In the proposed process, the wafer would first be subjected to a sacrificial oxidation to clean the surface. This sacrificial wet oxidation was performed both on the 6H-SiC and 4H-SiC wafer, as well as a monitor 6H-SiC wafer. The wafers were first subjected to an RCA clean (5 minutes in $NH_4OH:H_2O_2:H_2O$::1:1:5 at 75°C followed by a 5 minute rinse followed by 5 minutes in $HCl:H_2O_2:H_2O$::1:1:5 at 75°C followed by a 5 minute rinse) with no subsequent BOE dip. The wafers were then subjected to dry-wet-dry oxidation for 5-240-5 minutes at 1100°C. The resultant oxide thicknesses were ellipsometrically measured using a Gaertner ellipsometer. The 6H-SiC wafer had a mean oxide thickness of 266A with a standard deviation of 3.3A and the 4H-SiC wafer had a mean oxide thickness of 311A with a standard deviation of 4.4A. The mean oxide thickness on the monitor 6H-SiC wafer was 267A with a standard deviation of 8.1A.

A low temperature oxide (LTO) of thickness 7000A was then be deposited on the wafer. This LTO acts as a mask for the subsequent implant step. Subsequent to patterning this layer of LTO, a further 1000A of LTO was deposited to act as a pad oxide during the source implant to keep the maximum dopant concentration at the surface and not inside the semiconductor. A two step N+ implant was performed at MCNC (dose=2x1015 cm-2: energy = 80keV :: dose= 1×1015 cm-2: energy = 40keV). While the mean thickness of the first LTO layer can have

some variability since its only function is to act as an implant mask, the mean thickness of the second LTO layer must be very close to 1000A as the doses and energies of the subsequent implant steps have been designed and optimized taking into account a pad oxide thickness of 1000A.

The wafer was then subjected to a high temperature anneal at 1250°C for 30 minutes in argon + 1% oxygen to activate the dopant. The 1% oxygen is included to prevent the evaporation of Si during the argon anneal. The LTO was then further patterned to define the gate region and the gate dielectric thermally grown on the SiC. The thermal oxidation conducted in pyrogenic steam at 1100°C for 240 minutes with a 5 minute dry oxidation preceding it. The oxidation temperature was then reduced to 900°C and further wet oxidation was performed for 30 minutes. A final 5 minute dry oxidation step was performed before ramping down in N_2 to the furnace idling temperature of 750°C.

A blanket deposition of silicon was then done after performing an RCA clean on the wafers. The thickness of the silicon, which was amorphous was measured using Nanometrics and found to be 4200A with a variation of 5%. The wafers were cleaned again with a RCA clean and heavily doped N+ with phosphorus disks at 900°C for 30 minutes. This converted the amorphous silicon into polysilicon. The sheet resistivity of the poly was measured using a 4 point probe to be around 31 W/o. This is satisfactorily low.

The first level of the Mask set was used to define the area receiving the N+ nitrogen implant required for the source regions of the MOS-gated diodes. The second level of the Mask set was used to define the area of the SiC on which the gate oxide would be thermally grown or deposited. In other words, this level would act as the active area mask. These two levels have been completed. The third level of the Mask set will be used to define the polysilicon gate regions and the fourth level of the Mask set will be used to define the metal regions for contacts and pads. The processing of the third level has been delayed by a few days due to a problem with the RIE system which is used to pattern the poly. Only about 20 steps remain to be completed in the process including the metallization steps and, hence, these will be completed soon.

C. Conclusions

A Mask set was been designed to fabricate devices that would enable accurate characterization of the SiO_2-SiC interface. Devices that will be fabricated include MOS capacitors and MOS gated diodes. The wide band-gap of SiC and the attendant modifications that this fact introduces in the characterization of the interface as opposed to the characterization of the SiO_2-Si interface have been recognized. The Mask set was delivered and various preliminary experiments were conducted to ensure that the fabrication steps conform to the requirements of the process. The fabrication process was commenced and the N+ implant and

active area regions have been defined. The gate regions and the metal contacts remain to be defined and these will be done shortly.

D. Future Research Plans and Goals

The fabrication will be completed as speedily as possible and the characterization of the oxide films started.

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